New MISO-Type Universal Biquad Employing a Minimum Number of All Grounded Passive Elements

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This paper presents a new multiple-input single-output (MISO) type current-mode universal biquad which can realize all the five basic filter functions using only two Differential Difference Current Conveyors (DDCCs) and a minimum number of grounded passive elements. The workability of the new configuration has been verified by PSPICE simulation results based upon a CMOS DDCC in 0.35 μm technology.

Keywords:

Current conveyor, biquad filters, analog circuit design, current- mode circuits.

1. INTRODUCTION

The Differential Difference Current Conveyor (DDCC) has been found to be an attractive and flexible building block in realizing various signal processing and signal generation circuits, for instance, see [1]-[10]. Recently, Chen and Chu (see [1]) presented a new versatile voltage-mode multifunction active biquad filter employing DDCCs. This circuit can operate in single input multi output (SIMO) mode as well as multi input single output mode (MISO) and employs a minimum number of two resistors and two capacitors. However, since one of the resistors used therein is floating, the circuit does not have both grounded resistors which is desirable when electronic control of filter parameters is intended because such grounded resistors can be readily replaced by FETs/MOSFETs operated as voltage controlled resistors.

The main objective of this communication is to present a new circuit which, like the circuit of [1] employs exactly the same number of active components (two DDCCs) and passive components (only two resistors and two capacitors) but, in contrast to the circuit of reference [1] (which realizes voltage mode (VM)-functions), realizes all the five basic filter functions in current-mode with the advantage of employing all grounded passive components.

2. PROPOSED CONFIGURATION

The proposed MISO-type current-mode universal biquad configuration is shown in Figure 1.

Assuming the DDCCs to be characterized by:

$$\begin{bmatrix} V_x \\ I_{Y1} \\ I_{Y2} \\ I_{Y3} \\ I_z \end{bmatrix} = \begin{bmatrix} 0 & 1 & -1 & 1 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ \pm 1 & 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} I_x \\ V_{Y1} \\ V_{Y2} \\ V_{Y3} \\ V_z \end{bmatrix} \quad (1)$$

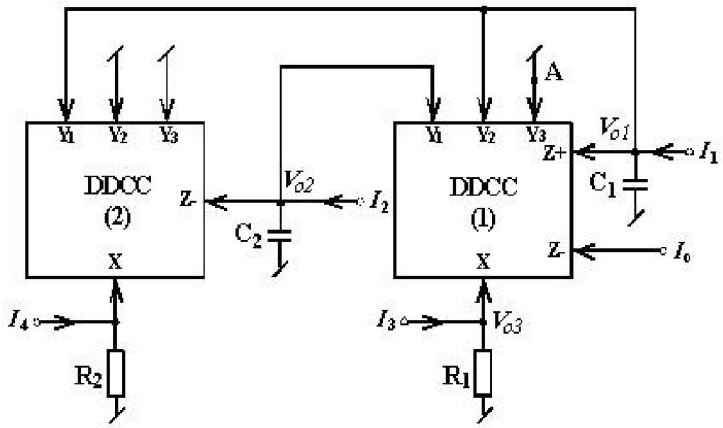


FIGURE 1 The proposed configuration

a straight forward analysis of the circuit reveals the following expression of the output current I_o in terms of the four input currents I_1, I_2, I_3 and I_4:

$$I_o = \frac{-I_3 s^2 C_1 C_2 + (I_2 + I_4) s C_1 G_1 - I_1 (s C_2 G_1 + G_1 G_2)}{s^2 C_1 C_2 + s C_2 G_1 + G_1 G_2} \quad \text{where } G_i = 1/R_i \text{ ; } i = 1 - 2 \qquad (2)$$

The various filter types can be realized from the circuit of Fig. 1 as follows:

LPF: (i) making $I_3 = I_4 = 0$, $C_1 = C_2$ and taking $I_2 = I_1 = I_{in}$

or (ii) making $I_3 = I_2 = 0$, $C_1 = C_2$ and taking $I_4 = I_1 = I_{in}$

In both the cases, the resulting transfer function is given by

$$\frac{I_o}{I_{in}} = \frac{-1}{\Delta}(G_1 G_2) \qquad \text{where } \Delta = s^2 C_1 C_2 + s C_2 G_1 + G_1 G_2 \qquad (3)$$

BPF: (i) making $I_1 = I_3 = I_4 = 0$, and taking $I_2 = I_{in}$

or (ii) making $I_1 = I_2 = I_3 = 0$, and taking $I_4 = I_{in}$

thereby resulting in

$$\frac{I_o}{I_{in}} = \frac{1}{\Delta}(s C_1 G_1) \qquad (4)$$

HPF: making $I_1 = I_2 = I_4 = 0$ and taking $I_3 = I_{in}$ gives

$$\frac{I_o}{I_{in}} = \frac{-1}{\Delta}(s^2 C_1 C_2) \qquad (5)$$

Notch: (i) making $I_4 = 0$, $C_1 = C_2$ and taking $I_2 = I_1 = I_3 = I_{in}$
or (ii) making $I_2 = 0$, $C_1 = C_2$ and taking $I_4 = I_1 = I_3 = I_{in}$ gives a notch response characterized by

$$\frac{I_o}{I_{in}} = \frac{-1}{\Delta}\left(s^2 C_1 C_2 + G_1 G_2\right) \qquad (6)$$

APF: making $C_1 = C_2$ and taking $I_1 = I_2 = I_3 = I_4 = I_{in}$, an all pass function results which is given by

$$\frac{I_o}{I_{in}} = \frac{-1}{\Delta}\left(s^2 C_1 C_2 - sC_2 G_1 + G_1 G_2\right) \tag{7}$$

Thus, it is seen that the proposed circuit can realize all the five generic filter responses.

The various parameters of the realized filters are given by:

$$\omega_o = \sqrt{\frac{1}{C_1 C_2 R_1 R_2}} \quad ; BW = \frac{1}{C_1 R_1};\ Q_o = \sqrt{\frac{C_1 R_1}{C_2 R_2}} \tag{8}$$

$$\text{and } Ho = \begin{cases} \dfrac{C_1}{C_2}\, for BPF \\ -1,\ for LPF / HPF / Notch / APF \end{cases} \tag{9}$$

where ω_o = cut-off frequency in radian/sec, BW = bandwidth, Q_o = quality factor and H_o= gain factor.

It may be noted that the first DDCC is used almost like a normal CC whereas the second one has two *Y* inputs and two *Z*-outputs thereby requiring some what larger number of transistors than the former. However, this is more than compensated by the advantage of the use of a minimum number of passive components and the versatility of the circuit in realizing all the five standard filters.

It may be mentioned that an additional circuitry e.g. a multiple output current follower will be needed at the front end of the proposed CM filter circuits to realize the conditions of the kind $I_2 = I_1 = I_{in}$ but this feature is common to all MISO-type universal CM biquads published previously too (see [15] and the references cited therein) although none of the earlier workers have explicitly acknowledged this. Hence, the requirement of the

additional circuitry mentioned here should not be considered to be a handicap or additional requirement only for the proposed new circuit.

It is also interesting to note that the circuit of Figure 1 can simultaneously realize low pass, band pass, and high pass in voltage mode too if input-voltage V_{in} is applied at terminal (A) by ungrounding it and the outputs V_{o1}, V_{o2} and V_{o3} are taken from the nodes where I_1, I_2 and I_3 (which are not needed now) were injected earlier. The three voltage-mode filter responses which can be realized from the transformed form of the proposed circuit of Figure 1 are found to be:

$$\text{LPF: } \frac{V_{o2}}{V_{in}} = \frac{-1}{\Delta}\left(G_1 G_2\right) \tag{10}$$

$$\text{BPF: } \frac{V_{o1}}{V_{in}} = \frac{1}{\Delta}\left(sC_2 G_1\right) \tag{11}$$

$$\text{HPF: } \frac{V_{o3}}{V_{in}} = \frac{1}{\Delta}\left(s^2 C_1 C_2\right) \tag{12}$$

where Δ and the relevant filter parameters remain same as in equations (3), (8) and (9).

3. NON-IDEAL ANALYSIS

We now consider the non-idealities of a DDCC using the following nonideal characteristics: $V_X = \beta_a V_{Y1} - \beta_b V_{Y2} + \beta_c V_{Y3}$ and $I_Z = \pm \alpha I_X$ where $\alpha_i = (1 - e_i)$ and e_i ($|e_i| \ll 1$) denote the current tracking errors and $\beta_v = (1 - e_v)$ and e_v ($|e_v| \ll 1$) denote the differential voltage tracking errors.

The non-ideal expression for the output current of the circuit of Figure 1 is found to be

$$I_0 = \frac{-I_3 s^2 \alpha_1 + (I_2 + \alpha_2 I_4) s \frac{\alpha_1 \beta_{a1}}{C_2 R_1} - I_1 \left(s \frac{\alpha_1 \beta_{b1}}{C_1 R_1} + \frac{\alpha_1 \alpha_2 \beta_{a1} \beta_{a2}}{C_1 C_2 R_1 R_2} \right)}{s^2 + s \frac{\alpha_1 \beta_{b1}}{C_1 R_1} + \frac{\alpha_1 \alpha_2 \beta_{a1} \beta_{a2}}{C_1 C_2 R_1 R_2}} \quad (13)$$

where (α_1 , β_{a1} and β_{b1}) belong to the first DDCC and (α_2 and β_{a2}) belong to the second DDCC. The non-ideal expressions for ω_o and Q_o are found to be:

$$\omega_o = \sqrt{\frac{\alpha_1 \alpha_2 \beta_{a1} \beta_{a2}}{C_1 C_2 R_1 R_2}}, \; Q_o = \frac{1}{\beta_{b1}} \sqrt{\frac{\alpha_2 \beta_{a1} \beta_{a2} C_1 R_1}{\alpha_1 C_2 R_2}} \quad (14)$$

The non-ideal gains and realization conditions (wherever applicable) get modified as follows:

H_{0LP} = -1; where the condition of realization modifies to $\beta_{b1} C_2 = \beta_{a1} C_1$ when $I_2 = I_{in}$ or $\beta_{b1} C_2 = \alpha_2 \beta_{a1} C_1$ when $I_4 = I_{in}$.

$H_{0BP} = \frac{\beta_{a1} C_1}{\beta_{b1} C_2}$ when $I_2 = I_{in}$ or $\frac{\alpha_2 \beta_{a1} C_1}{\beta_{b1} C_2}$ when $I_4 = I_{in}$.

$H_{0HP} = - \alpha_1$.

H_{0Notch} = -1, if $\alpha_1 = 1$; realization condition being the same as in LP.

H_{0AP} = -1, if $\alpha_1 = \alpha_2 = 1$ and $\beta_{b1} C_2 = \beta_{a1} C_1$

From the above, the active and passive sensitivities of the non-ideal ω_o and Q_o are found to be:

$$S_{C_1}^{\omega_o} = S_{C_2}^{\omega_o} = S_{R_1}^{\omega_o} = S_{R_2}^{\omega_o} = -1/2, S_{\alpha_1}^{\omega_o} = S_{\alpha_2}^{\omega_o} = S_{\beta_{a1}}^{\omega_o} = S_{\beta_{a2}}^{\omega_o} = 1/2, S_{\beta_{b1}}^{\omega_o} = 0$$
$$, S_{\beta_{b1}}^{Q_o} = -1, \quad S_{C_1}^{Q_o} = S_{R_1}^{Q_o} = S_{\alpha_2}^{Q_o} = S_{\beta_{a1}}^{Q_o} = S_{\beta_{a2}}^{Q_o} = 1/2,$$
$$S_{C_2}^{Q_o} = S_{R_2}^{Q_o} = S_{\alpha_1}^{Q_o} = -1/2 \quad (15)$$

Since the active and passive sensitivities of ω_o and Q_o are found to be in the range $-1 \le S_x^F \le 1/2$, the circuit, thus, enjoys low sensitivities.

An alternative non-ideal analysis of the proposed circuit has also been carried out including the various parasitic impedances of the DDCCs. The resulting expressions are quite complex, hence, to conserve space, we present only the non-ideal expressions for ω_o and Q_o which are as follows:

$$\omega_o' = \sqrt{\frac{1}{C_1'C_2'}\left\{g_1g_2 + \frac{G_1'}{G_2''}g_2 + \frac{G_1'G_2'}{G_1''G_2''}\right\}} \qquad (16)$$

$$Q_o' = \frac{\sqrt{C_1'C_2'G_2''\left\{g_1g_2G_1'' + G_1'g_2 + \frac{G_1'G_2'}{G_2''}\right\}}}{C_1'G_1''g_2 + C_2'G_1''g_1 + C_2'G_1'} \qquad (17)$$

where $C_1' = C_1 + C_{Yb1} + C_{Yb2} + C_{Z1+}$, $C_2' = C_2 + C_{Ya1} + C_{Z2-}$, $G_1' = G_1 * g_{X1}$, $G_1'' = G_1 + g_{X1}$, $G_2' = G_2 * g_{X2}$, $G_2'' = G_2 + g_{X2}$, $g_1 = g_{Yb1} + g_{yb2} + g_{Z1}$ and $g_2 = g_{Ya1} + g_{Z2-}$, where C_{Ya1}, C_{Yb1}, C_{Ya2}, C_{Z1+}, C_{Z2-}, g_{Ya1}, g_{Yb1}, g_{Ya2}, g_{Z1+}, g_{Z2-}, g_{X1} and g_{X2} are the parasitic capacitors and conductances of the terminals Y_a, Y_b, Y_c, $Z\pm$ and X for DDCCs.

One can easily see that when external RC elements are selected such that ($C_1 >> C_{Yb1} + C_{Ya2} + C_{Z1+}$, $C_2 >> C_{Ya1} + C_{Z2-}$, $g_{X1} >> G_1$ and $g_{X2} >> G_2$), the above expressions become almost same as their ideal counterparts.

To get a quantitative assessment of the amount of errors introduced by the parasitics, it is found that with $C_1 = C_2 = 31$pF, $R_1 = 26$kΩ, $R_2 = 1$kΩ and the parasitic elements taken as $r_{X1} = r_{X2} = 47$Ω, $r_{Z1+} = r_{Z2-} = 2.2$MΩ, $C_{Ya1} = C_{Yb1} = C_{Ya2} = C_{Z1+} = C_{Z2-} = 0.2$pF and $r_{Ya1} = r_{Yb1} = r_{Ya2} = 2.2$MΩ [2], the non-ideal values of

the parameters are found to be ω_o' = 6082100 rad/s and Q_o' = 4.7256 against their ideal values of ω_o = 6326300 rad/s and Q_o = 5.099 which shows the errors to be around 3.86% and 7.62%, respectively.

3. SPICE SIMULATION RESULTS

To verify the validity of the various function realizable from the proposed configuration, SPICE simulation of the proposed current mode filters has been carried out using the CMOS DDCC implementation taken from [3], reproduced here in Figure 2.

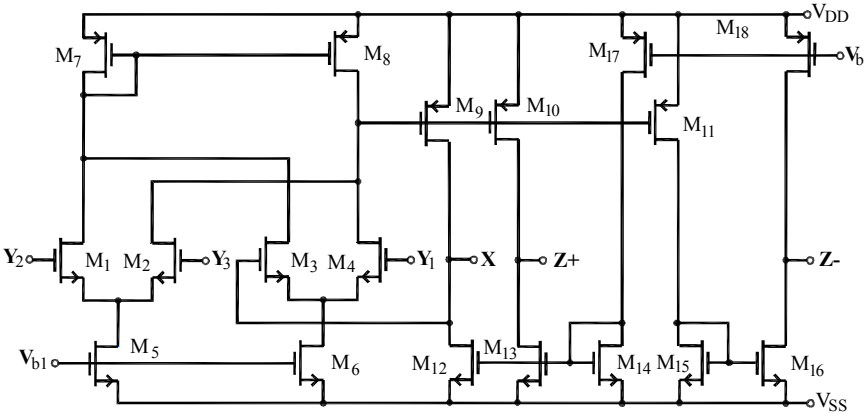


FIGURE 2 The CMOS implementation of a DDCC

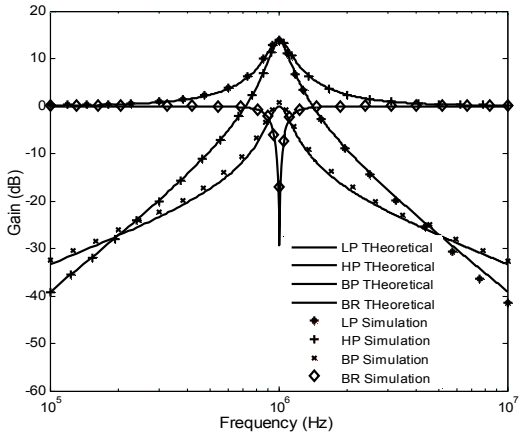
The model parameters of n-channel and p-channel MOSFETs have been taken corresponding to 0.35 μm CMOS technology, whereas aspect ratios of the MOSFETs were taken to be as shown in Table 1.

Table 1: Aspect ratios of MOSFETs.

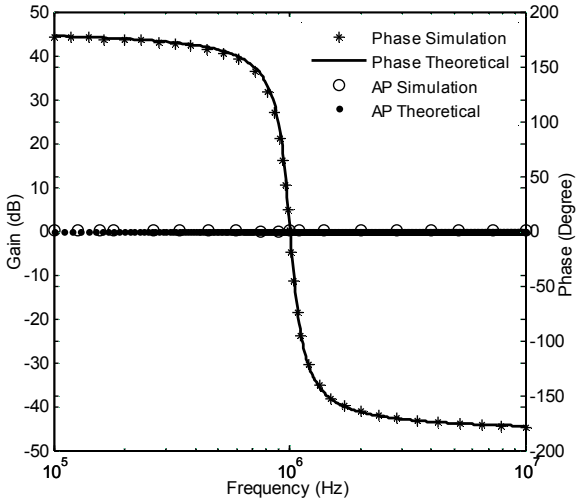
MOS transistors	W/L
M1- M4	0.75/0.35
M7, M8	15/0.75
M9 - M11, M17 - M18	10/0.4
M5, M6, M12 - M16,	5/1.15

The CMOS DDCC was biased with DC power supply voltages V_{DD}= +1.5V and V_{SS} = −1.5V and the biasing voltages

were taken as V_b = - 0.55V, and V_{b1} = 0.55V. To achieve the filters parameters f_o = 1MHz and quality factor of Q_o = 5.1, the component values were selected as R_1 = 26kΩ, R_2 = 1kΩ, and C_1= C_2 = 31pF. The frequency responses of LPF, BPF, HPF, Notch and APF are shown in Fig 3 which shows a very good correspondence between designed values and values determined from PSPICE simulations.



(a)



(b)

FIGURE 3 PSPICE Simulation results (a) Magnitude responses of LPF, BPF, HPF and Notch (b) Magnitude and Phase response of APF

To test the input dynamic range of the proposed filters, the simulation of the band-pass filter has been carried out with a sinusoidal input signal by designing the filter for f_o = 1 MHz, Q_o = 1 with component values taken as $R_1 = R_2$ = 5.1 kΩ. Figure 4 shows that the input dynamic range of the filter response extends up to amplitude of 100 μA without significant distortion. The dependence of the output harmonic distortion on the input signal amplitude is illustrated in Figure 5. For input signal amplitudes lower than 115 μA, the total harmonic distortion was found to be less than 4 %. The simulation results show that the circuit operates properly even at signal amplitudes of about 115 μA. The SPICE simulation results of Figure 3-5, thus, confirm the practical viability of the proposed configuration of Figure1.

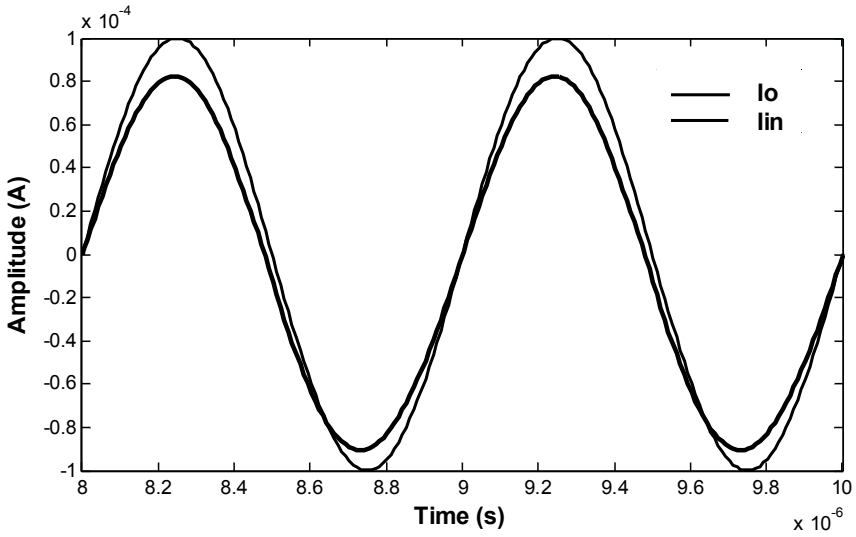


FIGURE 4 The input and output waveforms of the proposed band-pass filter of the proposed circuit for sinusoidal input current of 100 μA, 1MHz

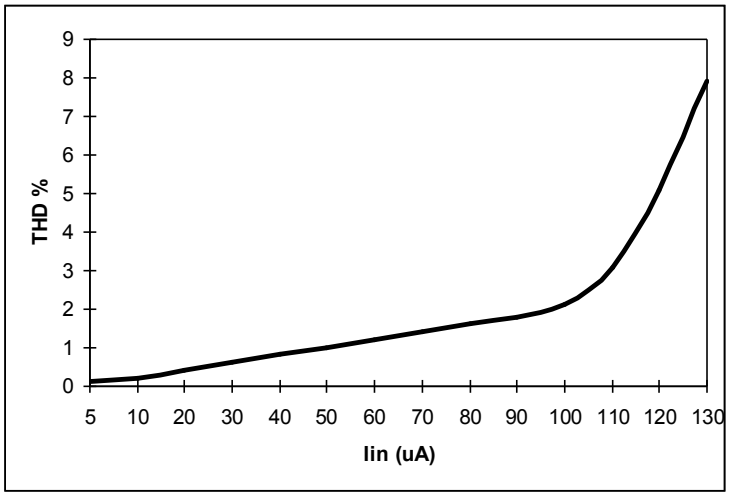


FIGURE 5 Dependence of output current harmonic distortion on input current amplitude of the band-pass filter of proposed circuit.

5- CONCLUDING REMARKS

In this paper, a new universal biquad current-mode MISO-type filter circuit has been proposed and its workability has been confirmed by PSPICE simulation results based upon a CMOS DDCC in 0.35μm technology. A comparison with some relevant earlier circuits of [1, 12-16] is now in order.

A comparison with MISO type universal voltage mode biquad using DDCCs, presented recently in [1] (Figure 1, case III therein) shows that whereas the quoted circuit of [1] has one floating resistor in case of LPF and HPF and two floating resistors in case of Notch and APF, the proposed circuit in Fig.1 has no floating passive elements in any of the five filter functions and uses only grounded passive elements which makes the proposed circuit suitable for IC implementation [11]. With appropriate changes, the circuit can also realize LPF, BPF and HPF in voltage mode.

When compared with the MISO-type CM biquads using current conveyors proposed earlier in [12]-[14], it is seen that the

proposed circuit uses one less resistor than the circuit of [12] and requires one active element less than the circuits of both [13] and [14]. Because of employing two DDCC and only four passive elements the circuit may be compared with some of the earlier works for instance[16] which also use exactly same number of active and passive elements. In this context, however, it may be noted that the circuit of Fig.2 of [16] is essentially two input-two outputs biquad as opposed to MISO-type structure proposed here.

Lastly, it must be mentioned that it has came to our attention only recently that a some what similar circuit had been reported earlier in [15], however, development of the circuit has been carried out independently. In fact, I was unaware of the existence of the quoted paper of the time of carrying out the present work. In view of this, a comparison of the proposed circuit of Figure 1 with that of [15] need to be done carefully. In this context, the following may be noted: (i) The circuit of [15] can operate in MISO-type current mode and MISO as well as SIMO-type voltage mode (ii) it employs four resistors and two capacitors (iii) This circuit suffers from the drawbacks of connection of capacitors at terminal X of CCs which may make the circuit unstable (iv) in MISO-type current mode (Part III therein), the circuit uses three resistors, however, since one of the resistors used therein is floating, the circuit does not have all grounded resistors (v) the circuit has matching condition ($G_1= G_2= G_3$) for realizing APF (vi) in SIMO-type voltage mode, the first circuit (Part II therein) uses two resistors one of which is floating and finally, (vii) the second circuit (Part V therein) would become same as my circuit of figure 1 if RC-CR transformation is applied on this quoted version of the circuit of [15].

From (i) – (vii) above, it is clear that my circuit of Figure 1 is not exactly similar to that of [15] and hence, is ‘justifiably’ a new configuration.

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