

Synthesis of FC-OTA and CMOS CFOA Using Super Buffer Technique

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Abstract:-

A new design technique employing super buffer stage in the simulation of Current Feedback Operational Amplifier (CFOA) is presented. The super buffer stage is connected in the output node of high performance Folded Cascode OTA (FC OTA) that represent the input stage of CMOS CFOA. The performance parameters of CMOS CFOA such as bandwidth, slew rate, settling time are extensively improved compared to traditional buffer stage. These parameters are very important in high frequency applications that use CMOS CFOA as an active building block such as A/D converters, and active filters. Also the DC input offset voltage and harmonic distortion (HD) of very low values compared with the conventional CMOS CFOA are obtained. P-Spice simulation results using 0.5 μm MIETEC CMOS process parameters shows considerable improvement over existing CMOS CFOA simulated model using traditional buffers. Some of the performance parameters for example are DC gain of 67.2 dB, open-loop gain bandwidth product of 104 MHz, slew rate (SR+) of +91.3V/ μS and DC input offset voltage of -0.2mV.

Keywords: Synthesis of FC-OTA and CMOS CFOA; super buffer technique, high performance CFOA, Low input offset voltage CFOA, low distortion CFOA.

1. INTRODUCTION

The current feedback operational amplifier (CFOA) is gaining in importance as a building block in electronic circuit design. It is fundamentally a transimpedance amplifier and achieves high transfer function accuracy, low distortion and wide bandwidth because of the current feedback applied around it. Its basic circuit topology results in a high slew rate as well as a constant bandwidth feature (bandwidth gain independence) that is quite attractive [1]. Advances in bipolar process (especially in terms of complementary performance of transistors npn and pnp) and the inherent better current-drive capability, leave BJTs as the most suitable device for the implementation of CFOAs. Several CFOA designs from commercial manufactures are available. Recently, CMOS architectures have also been presented that focused on a particular performance parameters [2]. However, the conventional CMOS CFOA design is still facing certain problems, first, the offset voltage on the current feedback can not be made zero. CFOA usually adopts an analog buffer as the input stage. As a result, the non-inverting input has very high impedance, while the inverting input has very low impedance. Hence, the CFOAs offset is higher than VFA Design. Second, the constant bandwidth feature of the CFOA is only approximate if the inverting input impedance is not small enough [3]. The low-input offset voltage is considered as an important aspect of the performance of an amplifier especially when signals are in the range of few hundred micro volts [4]. Several CMOS realizations for the CFOA have been reported in the literature [5]-[12]. In Jirauth M. and Chris T.[5] present a detailed stability analysis of the CFOA in high frequency operation. Two CMOS CFOA for high drive capability utilize class AB differential amplifiers in unity feedback, there by allowing high slew rate values and relatively low input/output resistance to be achieved in Giuseppe Di Cataldo and etal [6]. A new CMOS CFOA with an on-chip current-mode input offset voltage compensation circuit proposed by Ali Assi and etal [7]. A novel realization of

the CFOA is presented in Aly M. and et al [8]. The architecture, current mirrors are completely avoided and high accuracy is obtained by merging all the terminals in one feedback-stabilized structure. Wide bandwidth CMOS CFOA for inverting applications proposed by S. Selvanayagam and F.J.Lidgey [9]. This realization apply negative feedback around the input stage to decrease input resistance and a consequence larger bandwidth of operation at high closed loop is gained. A CMOS CFOA with a novel on-chip current-mode input offset voltage compensation circuit proposed by Jieyan Zhu and et al [10]. To make the compensation effective of CFOA, circuit of art BJT based a folded cascode voltage operational amplifier (VOA) is considered by G. Palumbo and S. Pennisi [11]. A simple compensation circuit to reduce the offset voltage is proposed by M. Djebbi and et al [12]. The design still suffers from many drawback such as high distortion, high noise, high consumption of power and complex circuitry. This paper describes an alternative approach to CMOS CFOA design which provides symmetrical high impedances (infinite for DC) inputs together with high performance parameters in high frequency operation. This design approach apply CMOS folded cascode OTA as input stage along with super buffer stage as output stage connected to high output impedance node of FC OTA which represent the transimpedance node of CMOS CFOA. This synthesis of FC OTA and CMOS CFOA combine the high performance parameters of high frequency operation, low DC offset voltage and low harmonic distortion. The primary advantage of FC OTA is that the frequency response, slew rate and settling time can be improved since the phase shift of extra stage is eliminated, and reduced power consumption. In addition to that the symmetrical input stage will reduce the DC offset voltage of CMOS CFOA. Moreover the asymmetry of the conventional buffer stage is clearly undesirable and gives rise to significant delay problems when it is used to drive more significant capacitive loads. In addition to that the asymmetry is increases harmonic distortion. The super buffer stage works on

sources transistors. Transistors M3-M4 and transistors M7-M8 which are represents the load transistors of the input stage. The second stage is traditional source follower output stage which represented with transistors M13 and M14. For many front-end applications, such a structure suffers from a disadvantage of unsymmetrical input impedances,

which is not the case for VFA. In addition, only gains ≥ 1 can be adjusted [13] and gain changes requires tuning of the R_F resistor, which is more difficult to implement on a chip. Most of the front-end analog channels require symmetrical high input impedances (infinite for DC) and in many cases a gain of < 1 is also a necessity. This is why VFA is more popular even though the AC performance of CFOA is better. A relation between the input voltages of the amplifier is given by [4]:

$$V_{in}^- = V_{in}^+ + (V_{T1} - V_{T2}) + \left[\sqrt{\frac{I_{D1}}{\beta_1}} - \sqrt{\frac{I_{D2}}{\beta_2}} \right] \quad \text{-----(6)}$$

Eg. (6) shows that offset and distortion occur if threshold voltages, V_{Ti} or trans conductance factors, β_i , of the source coupled pair M1-M2 are affected by mismatch or if their drain currents are not equal [4]. The FC OTA does not require perfect balance of currents in the differential amplifier because excess dc current can flow into or out of the current mirror.

4. OERATION OF SUPER BUFFER STAGE

The asymmetry of the conventional inverter is clearly undesirable and gives rise to significant delay problems when an inverter used to drive more significant capacitive loads [17]. A common approach used to alleviate this effect and improve performance parameters of the proposed CMOS CFOA is to make use of super buffer technique as illustrated in Fig. 4.

The inverting type is shown in Fig. 4(a); Considering a positive is going logic transition V_{in} at the input, it will be seen

that the inverter formed by transistors M15 and M16 is turned on and, thus, the gate of M17 is cut off while M18 (the gate which is also connected to V_{in}) is turned on and the output is pulled down quickly. Now consider the opposite transition: When.

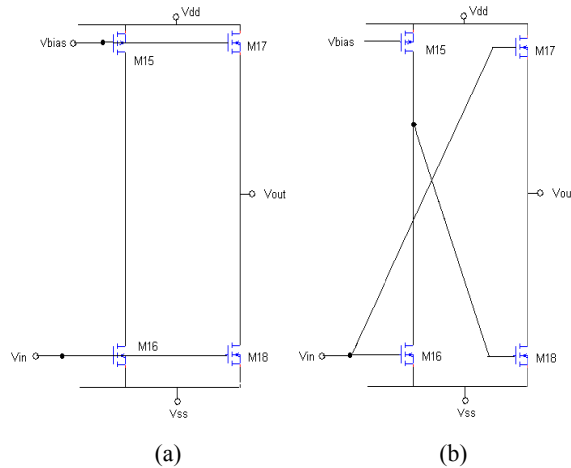


Fig. 4. Super Buffer stage (a) Inverting (b) Non inverting

V_{in} drop to 0 volt then the gate of M17 is allowed to rise quickly to V_{dd} . Thus, as M18 is also turned off by M17 is caused to conduct with V_{dd} on its gate, that is with twice the average voltage which would be applied if the gate was tied to the source as in the conventional inverter. Now, since $I_{ds} \propto V_{gs}$ then clearly, doubling the effective V_{gs} will increase the current and, thus, reduce the delay in charging any capacitance on the output. Thus, more symmetrical transitions are achieved [17]. The corresponding non-inverting super buffer stage is given in Fig. 4(b).

Remark: In case of analog input signal is applied the positive half cycle represents the transition to logic 1 volt in case of digital signal and negative half cycle of analog signal represents the transition to logic 0 volt.

4.1. DESIGN OF SUPER BUFFER STAGE

Super buffer stage consists of two parts, the first part is inverter stage represented by two transistors M15 and M16 as shown in Fig. 4. Hence, the aspect ratios of these transistors can be calculated by using the following equ. [15]:

$$I_d = \beta \frac{W}{L} (V_{GS} - V_T)^2 \quad (7)$$

For a biasing voltage ($V_{bias}=-1V$) and the dc current ($I_d=100\mu A$), then the aspect ratios are:

$$\left(\frac{W}{L}\right)_{15} = \frac{I_d}{\beta_P (V_{GS} - V_{TP})} \quad (8)$$

$$\left(\frac{W}{L}\right)_{16} = \frac{I_d}{\beta_N (V_{GS} - V_{TN})} \quad (9)$$

The second part of super buffer stage is a buffer stage, so that design of this stage depends on the same concepts that were discussed in section (3.1) since low output impedance and unity gain are required in this stage. Hence, the aspect ratios of this stage represented by the two transistors M17 and M18 are $(W/L)_{17} = 11.9$ and $(W/L)_{18} = 3.0$

5. DESIGN OF CMOS CFOA USING SUPER BUFFER STAGE

Fig. 5 shows the architecture of unconventional CMOS CFOA using super buffer stage as output buffer stage and based on the folded cascoded operational trans conductance amplifier FC OTA as input stage. This FC OTA uses cascoding in the output stage combined with an unusual implementation of the differential amplifier to achieve good input common-mode range. Thus, the folded cascode OTA offers self-compensation, good input common-mode range, and the gain of a two-stage OTA [15]. The FC OTA does not require perfect balance of currents in the differential amplifier because excess dc current can flow into or out of the current mirror. When the bias current and overdrive voltage of each

transistor is known, we can easily determine the aspect ratios from the following equation [15]:

$$I_D = (1/2)\mu C_{OX}(W/L)(V_{GS} - V_{TH})^2 \quad (10)$$

To minimize the device capacitances, we choose the minimum channel length for each transistor, obtaining a corresponding gate width. The design has thus far satisfied the output swing, power dissipation, and supply voltage specifications [18]. Let us now calculate the maximum output voltage swing of the CMOS CFOA in Fig. 5, where M_5 - M_6 , and M_9 - M_{10} represents current sources with proper choice of V_{b1} and V_{b2} , the lower end of the swing is given by: Lower end swing = $V_{SS} + V_{OD3} + V_{OD5}$ (11)

Upper end swing =

$$V_{DD} - (V_{OD5} + V_{OD3} + (|V_{OD7} + V_{OD9}|)). \quad (12)$$

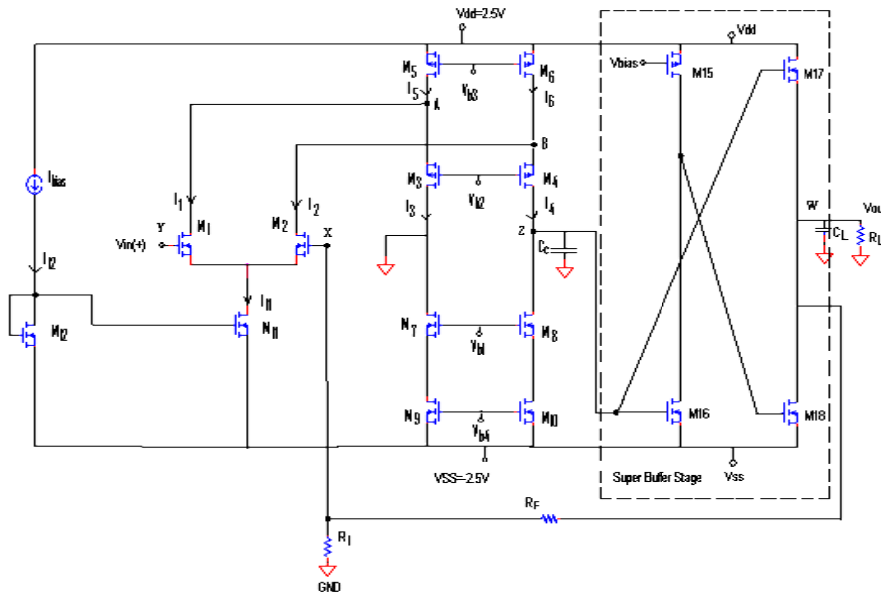


Fig. 5. Schematic circuit of CMOS CFOA using super buffer technique

In the CMOS CFOA circuit of Fig 5, the input CM level and the bias voltages must be chosen so as to

allow maximum output swing. Where M_5 - M_{10} represent the ideal current sources. Thus, the peak-to-peak swing on each side is equal to $V_{DD}-(V_{OD3}+V_{OD5}+|V_{OD7}|+|V_{OD9}|)$. We should nonetheless note that, carrying a large current, M_5 and M_6 may require a high overdrive voltage if their capacitance contribution to nodes A and B is not to be minimized. The supply voltages V_{DD} and V_{SS} of the proposed design are $\pm 2.5V$.

Table 1 Gate dimension and biasing currents of input stage of CMOS CFOA

Overdrive Voltage (V)	Biasing Current(uA)	L(um)	W(um)	Transistors No.
0.16	50.0	0.5	12.0	M1,M2
0.3	50.0	0.5	16.1	M3,M4
0.5	100.0	0.5	11.59	M5,M6
0.225	50.0	0.5	6.21	M7,M8,M9,M10
0.5	100.0	0.5	2.51	M11,M12
0.9	100	0.5	9.5	M15
0.29	100	0.5	2.0	M16
0.5	100	0.5	23.8	M17
0.42	100	0.5	6.0	M18

6. SIMULATION RESULTS

A new alternative CMOS CFOA with high performance operation, very low offset voltage and low distortion is proposed. Since, the high frequency parameters such as voltage gain, (-3dB) bandwidth, slew rate (SR), settling time(t_s) and gain bandwidth product (GBW) are improved. Fig.6 and Fig. 7 clarify the improvement in the open loop voltage gain and gain bandwidth product (GBW) of the CFOA used super buffer stage compared with CFOA used traditional buffer stage. The value of open loop gain bandwidth product (GBW) has doubled value

about 104MHz of the CFOA with super buffer stage compared with 54MHz of the CFOA used traditional buffer stage. The value of output impedance of buffer stage is decreased drastically due to using super buffer stage also. Fig. 10 and Fig. 11 shows the value of output impedance of CFOA used super buffer stage is 246 Ω and the value of output impedance of CFOA with traditional output stage is 5k Ω . Fig. 8 and Fig. 9 illustrated the improvement in closed loop (-dB band width) of the CFOA, since the values of (-dB bandwidth) is 79.6 MHz compared with 36.2 MHz with introduce the closed loop resistors are $R_F=1K\Omega$ and $R_I=1K\Omega$. DC characteristics of CMOS CFOA is shown in Fig. 12 and Fig. 13 we note that there is large enhancement in linearity of DC characteristics of the CMOS CFOA due to the symmetry in operation of the super buffer satge. Moreover, we note that the value of input offset voltage are low in both cases about 0.19mV, and -0.2mV as indicated in table 4, due to the symmetry in input stage (inverting and non inverting inputs) of the proposed CFOA. Table 2 and table 3 shows that when varies input resistors value (R_I) of the feedback loop gain and fixed the value of R_F (1k Ω) resistor of the CFOA the values of the closed loop voltage gain (A_v), gain bandwidth product (GBW),(-3dB) bandwidth, phase margin(PM), and total harmonic distortion(HD) will change according to simulation results that confirmed the theoretical equations in previous sections. Table 4 summarize the comparison of the performance parameters of the CFOA in Fig. 3 and CFOA in Fig. 5.

Table 2: Performance parameters of CMOS CFOA with traditional buffer stage

A_v dB	THD dB	PM deg	GBW MHz	-3dB B.W. MHz	RI K Ω
5.9	-63.0	80o	54.0	36.2	1
12.6	60.0	57o	40.5	13.5	0.3
20.5	41.0	56o	37.3	4.4	0.1
38.5	40.3	54o	36.8	0.55	0.01

Table 3: Performance parameters of CMOS CFOA with super buffer technique (SBT)

Av	THD	PM	GBW	-3dB B.W	RI
dB	dB	deg.	MHz	MHz	K Ω
5.9	-67.0	49.9o	104	79.6	1
12.5	-65.0	48.6o	89.2	32.7	0.3
20.4	-41.7	46.0o	81.8	10.7	0.1
39.1	-41.0	45.0o	78.6	1.0	0.01

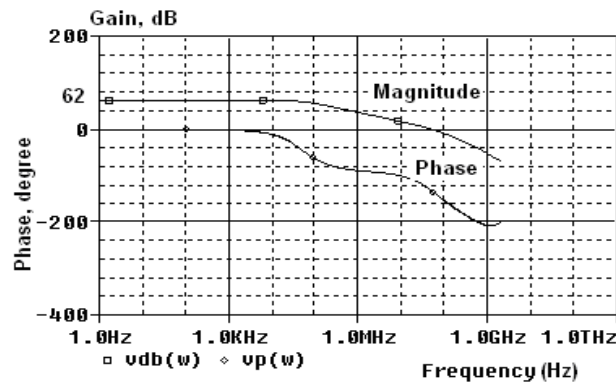


Fig. 6. Open-loop frequency response of CMOS

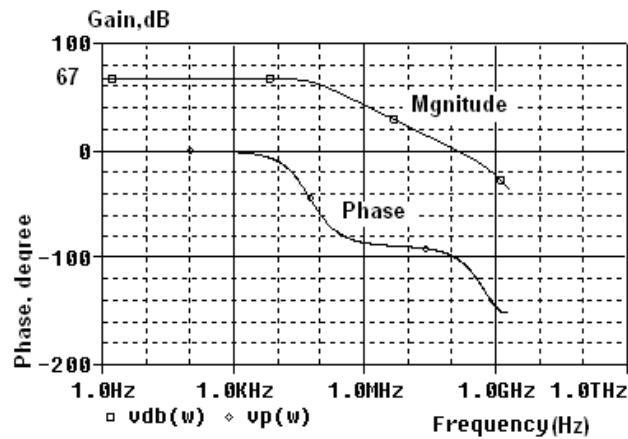


Fig. 7. Open-loop Frequency response of CMOS CFOA with Super buffer output stage

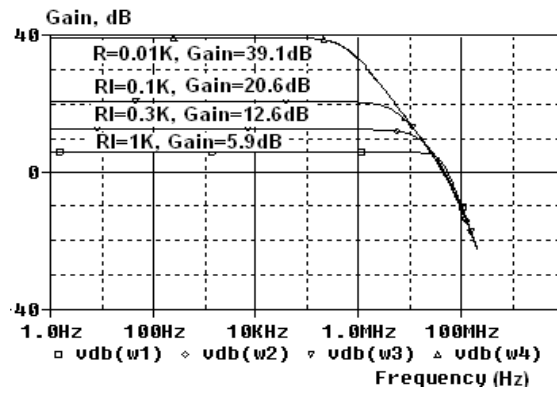


Fig. 8. Closed loop frequency response of CMOS CFOA with traditional output stage

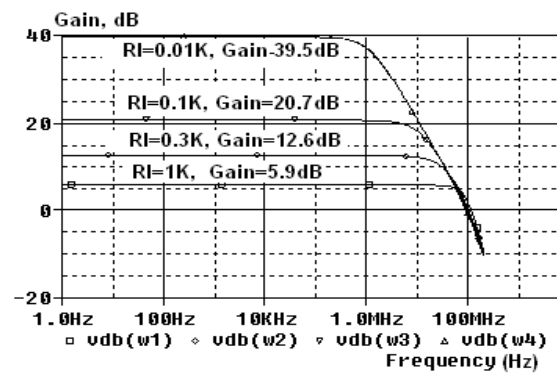


Fig. 9. Closed loop frequency response of CMOS CFOA with super buffer output stage

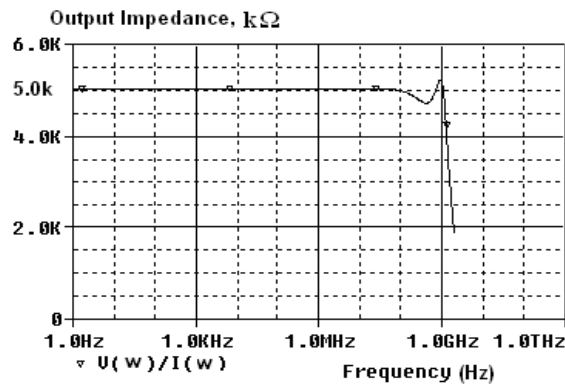


Fig. 10. Output impedance of the CMOS CFOA with traditional output stage

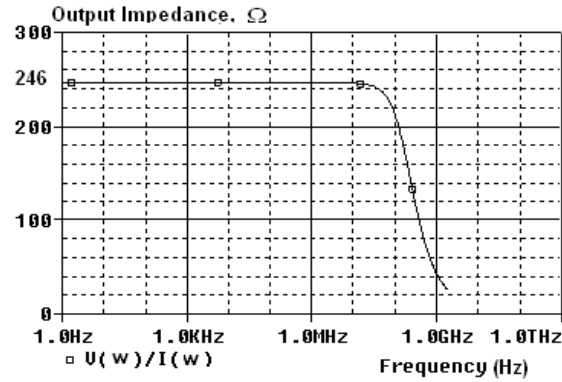


Fig. 11. Output impedance of the CMOS CFOA with super buffer output stage

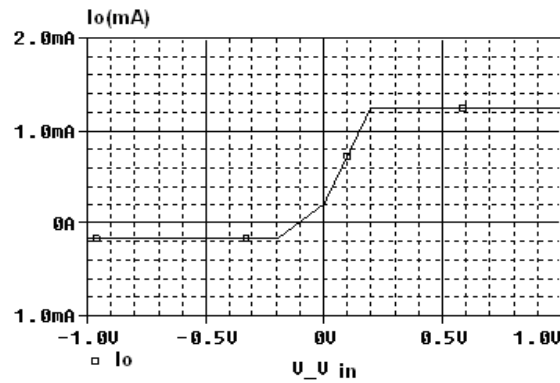


Fig. 12. DC characteristics of the CMOS CFOA with traditional output stage

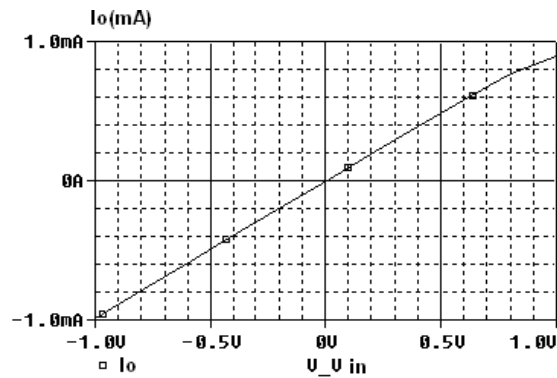


Fig. 13. DC Characteristics of the CMOS CFOA with super buffer output stage

Table 4: Summarize the performance parameters of the CFOA in Fig.3 and CFOA in Fig. 5

CMOS CFOA With super buffer technique (SBT) in Fig. 5	CMOS CFOA with traditional buffer stage in Fig. 3	Parameters
± 2.5	± 2.5	Supply voltage
100 μ A	100 μ A	Biassing current
Open loop results of the CMOS CFOA		
67.0dB	62.0dB	Open loop gain @RL=10K Ω , CL=10p
104MHz	54.0MHz	Open loop (GBW) at RL=10K Ω , CL=10pF
0.5pF	0.5pF	Compensation capacitor (Cc)
47 $^{\circ}$	53 $^{\circ}$	Phase Margin (PM)
156dB	156dB	Trans impedance gain at node (Z)
Closed loop results of the CMOS CFOA		
97.7MHz	46.0MHz	Closed loop (GBW) @RF = 1K Ω , RI = 1K Ω
79.6MHz	36.2MhZ	Closed loop (-3db) Bandwidth@ RF = 1K Ω , RI =1k Ω
49.9 $^{\circ}$	80 $^{\circ}$	Phase Margin (PM)
+92 V/ μ S, -89.0 V/ μ S	+71.2 V/ μ S, -61V/ μ S	Slew rate @ CL=10p
21 ns	46.0 ns	Settling time@ CL=10p
-67.0 dB	-63.0 dB	Total harmonic distortion(THD)
-0.2 mV	0.19 mV	Input offset voltage @Vin=0V
5.5 mW	4.0 mW	Consumption power
0.07 mm ²	0.052 mm ²	Die area

7. CONCLUSION

A new design of the CMOS CFOA with attractive features for high frequency, low offset voltage and low distortion is proposed in this paper. The proposed design based on super buffer stage that connected in the output stage of the folded cascade DO-OTA. Since this technique operate on logic transition concept which gives the high speed and symmetry operation of the output signal. The high speed operation improved high performance parameters such as gain bandwidth (GBW), (-3dB) bandwidth, slew rate (SR) and settling time (t_s) with ensure the phase margin (PM) in acceptable value that keep the stability of operation. Moreover, the symmetry of super buffer stage decreased the distortion in output signal and improved (DC) characteristics of CMOS CFOA. In addition to that using folded cascode OTA (FC-OTA) as the input stage of CMOS CFOA make the symmetry of inverting and non inverting inputs that reduce input offset voltage. The trans-impedance node (Z) of the CMOS CFOA gained high value due to cascoding transistors. This feature is very important for design CMOS CFOA with high gain. We can summarize our conclusion by saying that the proposed CMOS CFOA with symmetry of the input stage and symmetry of the output stage will gain CMOS CFOA attractive features for many high frequency, low distortion, low input offset voltage applications such as (A/D) converters, switched capacitor filters, active filters. In a nutshell it can be concluded that the proposed CMOS OTA is better compared to the earlier CMOS OTA schemes vis-à-vis frequency response and linearity.

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